RF and DC characteristics of low-leakage InAs/AlSb HFETs

B. Brar, G. Nagy, J. Bergman, G. Sullivan, and P. Rowell
Rockwell Scientific Company, Thousand Oaks, CA 91360

H. K. Lin, M. Dahlstrom, C. Kadow, and M. Rodwell
University of California, Santa Barbara, CA 93106

Abstract

InAs/AlSb HFETs with excellent RF and DC properties are reported. The drain currents are 750mA/mm with peak transconductance g_m of 1.1 S/mm. The gate leakage in is below 1nA/μm^2 for low gate bias. The threshold voltages of 0.25 μm and 0.5 μm gate-length devices are –2.5 and –1.5 V respectively, indicating short channel effects are present. Small-signal measurements on a 0.25 μm gate-length device show f_τ of 120 GHz and f_{max} of 100 GHz at drain voltages below 0.4V.

I. Introduction

Electrons in InAs/AlSb HFETs have high low-field mobility, high concentrations, and high peak and saturated velocities. A drawback of the technology is the low "breakdown" voltage associated with the relatively narrow bandgap InAs channel. As a result, InAs/AlSb HFETs are candidates for low-power high-frequency low-noise amplifiers and low-power high-speed digital ICs.[1] For such applications, we must design devices that exhibit high RF and DC performance at low drain and gate voltages. In the present work we report on the high quality characteristics of InAs/AlSb HFETs at drain biases below 0.4V.

II. Growth and Process Details

The InAs/AlSb HFET materials were grown by solid-state MBE on a semi-insulating (001) GaAs substrate. Valved cracker cells were used for both the Sb and the As beams. For Te doping, a PbTe source was used. The growth temperatures were calibrated with a pyrometer before starting the growth. Growth was initiated with a 0.1μm thick smoothing layer of GaAs and a 10nm thick transition layer of AlAs just before the nucleation of the 7% mismatched AlSb buffer layer. The AlSb buffer, grown at 570 °C, is 2μm thick and serves primarily to reduce the high density of threading dislocations to below 10^8 cm^{-2}. A 0.2 μm thick $Al_{0.8}Ga_{0.2}Sb$ layer was inserted prior to the growth of the InAs/AlSb HFET layers. The $Al_{0.8}Ga_{0.2}Sb$ layer provides a stable surface exposed during the mesa isolation fabrication step in the HFET process. The HFET active layers were grown at 500 °C and consisted of an 8nm thick AlSb bottom barrier, a 15nm thick InAs channel, and a 20nm thick AlSb top barrier. The InAs/AlSb interfaces are forced to be "In-Sb like" to provide the best transport properties

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for the InAs channel.[2,3] Tellurium modulation-doping of the top AlSb barrier is employed to supply the charge to the channel. The modulation doping layer is 3nm thick and separated from the InAs channel by a 5nm thick spacer. Finally, the layers are capped with a 5nm thick layer of $In_{0.5}Al_{0.5}As$. The energy band diagram for the device is shown in Figure 1. The $In_{0.5}Al_{0.5}As$ cap layer serves a dual purpose of protecting the underlying layers from oxidation and reducing gate leakage by increasing the valence band barrier between the channel and the surface.[1,4] Hall measurement on the as-grown wafer revealed a 300 K mobility of μ_e=16,000 $cm^2/V.s$ and an electron sheet concentration of N_s=5x12 cm^{-2}.

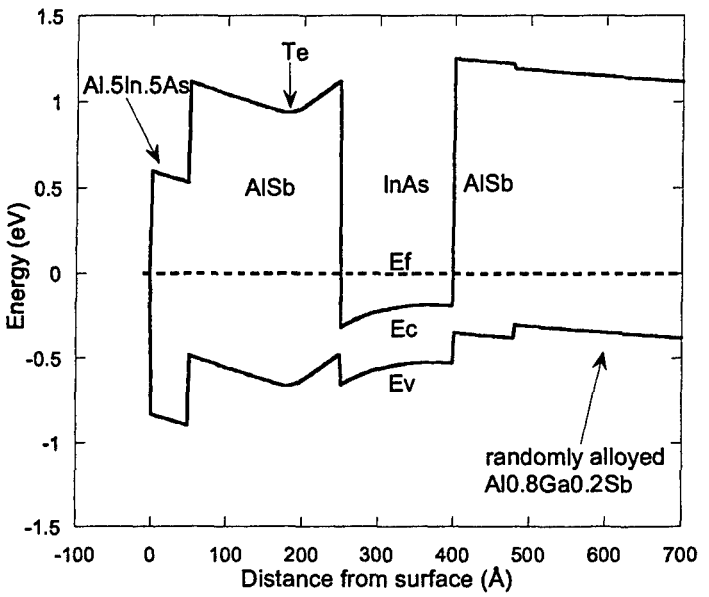

Figure 1. Energy band diagram of the InAs/AlSb HFET. The channel is modulation doped with Te donors in the top barrier and an $In_{0.50}Al_{0.50}As$ cap protects the AlSb barrier from oxidation and reduces gate leakage.

InAs/AlSb HFETs were fabricated using a conventional mesa-isolation process with alloyed Pd/Au contacts for the source and drain, and Cr/Au T-gates written with electron beam lithography. No gate-recess was required for these devices. Transmission-line measurements showed a contact resistance of 0.09 Ω-mm to the channel with a channel sheet resistance of 86 Ohms/square. The sheet resistance is consistent with the value obtained from the hall measurement. Devices with various gate-lengths and widths were written to understand the impact of these parameters on device operation.

III. Measurement and Results

The devices show typical output characteristics for InAs/AlSb HFETs with an enhanced drain conductance caused by impact ionization generated holes forward biasing the source-to-channel barrier.[5] We concentrate here on the input characteristics and the sub-threshold

characteristics of the device. Figure 2a shows the drain current and the transconductance g_m as a function of the gate voltage for an HFET with a gate length of 0.5μm. The drain current is a respectable value of 750 mA/mm at a drain voltage of 0.4V. The threshold voltage is -1.5V. The drain current changes only slightly at gate voltages close to zero volts thereby leading to lower g_m as may be expected for a device operating in the linear region. The g_m increases as the gate voltage is decreased and the device begins to operate in the saturated regime. We also note that the peak g_m increases dramatically as the *drain* voltage is increased peaking at a value over 1.1S/mm at a drain bias of 0.4V.

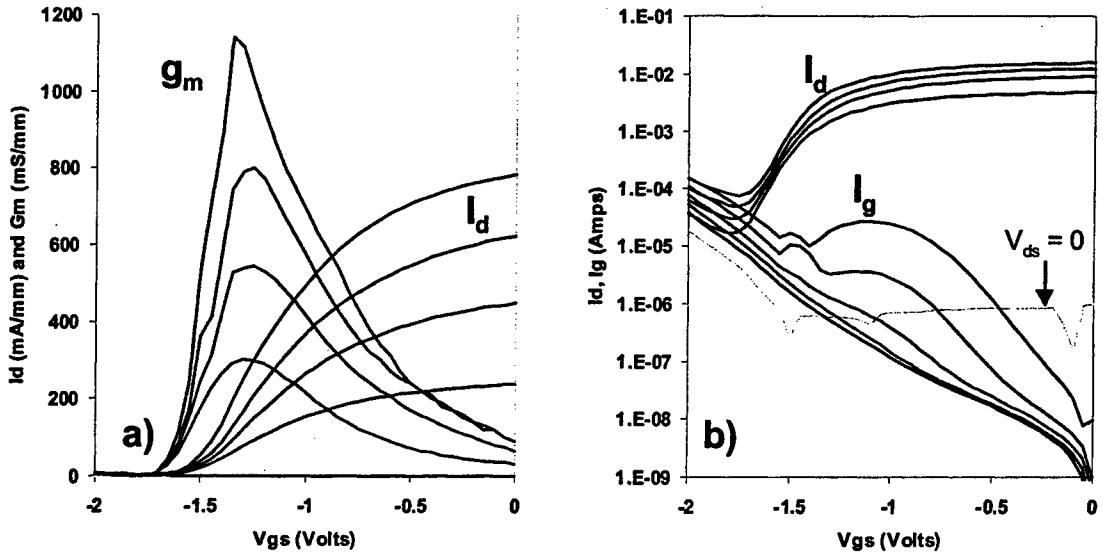

Figure 2 a) Drain current and DC transconductance g_m as a function of gate voltage for an HFET with a gate length of 0.5μm. The drain voltage is stepped at 0.1V with a maximum value of 0.4V. An I_{dss} of 750 mA/mm and $g_{m,max}$ of above 1.1 S/mm is excellent at these drain voltages. b) Sub-threshold characteristics of the same device showing very low gate leakage current below 10nA at low gate bias. The excess gate current at higher drain bias is a result of impact ionization in the channel. The dashed line is the drain current at 0V on the drain.

To further understand this increase in the g_m it is instructive to consider the sub-threshold characteristics of the device as shown in Figure 2b. The gate characteristics in Figure 2b show the previously observed excess gate current bumps associated with the collection of impact-generated holes by the negatively biased gate. The increase in g_m is commensurate with the excess gate currents. It appears that the dc g_m is artificially high due to the additional positive charge provided by the holes generated through impact ionization of hot electrons in the channel. The impact-generated holes are known to cause the increased output conductance in these devices, which simply translates into an inflated value for the transconductance.

A significant feature of our devices is their low-bias gate leakage of 1nA/μm^2, which is lower than the best published values for the InAs/AlSb HFETs. The low gate leakage is presumably a result of the $In_{0.5}Al_{0.5}As$ cap layer that presents a valence band barrier and reduces the leakage caused by hole conduction.[4] Devices with gate lengths of 0.25 μm were also characterized. The basic DC characteristics were largely similar with the exception of the threshold voltage, which was -2.5V compared to -1.5V for the 0.5 μm devices. This is the first indication that short channel effects (drain-induced barrier lowering) affect our present device design.

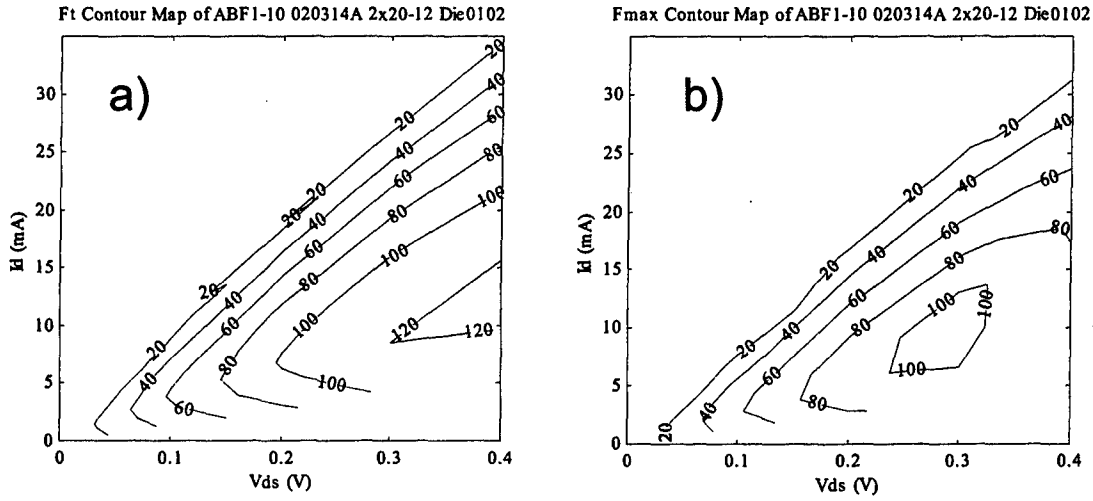

Figure 2 a) A contour plot of the small-signal current gain cutoff frequency f_τ for a 40μm wide InAs/AlSb HFET with a 0.25um gate length for a variety of gate and drain biases. b) A similar plot of the power gain cutoff frequency f_{max} for the same device. The pad parasitics have not been de-embedded from the small-signal data.

The RF characteristics of the devices were measured over a range of biases and contour maps of the RF parameters were generated as a function of dc bias. Figure 3 shows the contour maps for f_τ and f_{max} as a function of bias. For the 0.25 μm gate length HFET we obtain a peak f_τ of 120 GHz and f_{max} of 100 GHz for drain biases between 0.3V and 0.4V. The pad parasitics have not been de-embedded from the RF data. The devices exhibit poor RF performance at low gate biases, almost independent of the (relatively small range in) drain voltage. Given the high threshold voltages of these transistors, the lower f_τ and f_{max} at the low gate biases is a direct consequence of operating the device in its linear region. We also observe that the range in f_τ for these devices is considerably lower than the relative range of the dc g_m. The poor correlation between f_τ and dc g_m is consistent with our qualitative explanation that the anomalously high dc g_m reflects charge modulation from sources other than the input signal on the gate.

IV. Conclusions

The InAs/AlSb devices presented exhibit high drive current, low gate-leakage, excellent sub-threshold characteristics, and good RF properties. Sub-threshold measurements show gate currents below 1nA/μm^2 at low gate bias. Small-signal measurements on a 0.25 μm gate-length device demonstrate f_τ of 120 GHz and f_{max} of 100 GHz at drain voltages below 0.4V. The absolute threshold voltage for the present device design is high and must be increased above –1V for use in low-power high performance circuits.

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